ABSTRACT

[0066] A 2-terminal trapped charge memory device is disclosed with voltage switchable multi-level resistance. The trapped charge memory device has a trapped charge memory body sandwiched between two electrodes. The trapped charge memory body can be made of a variety of semiconducting or insulating materials of single-crystalline, poly-crystalline or amorphous structure while containing current carrier traps whose respective energy levels and degrees of carrier occupancy, modifiable by the height and width of an applied write voltage pulse, determine the resistance. The mechanism of modification can be through carrier tunneling, free carrier capturing, trap-hopping conduction or Frenkel-Poole conduction. The current carrier traps can be created with dopant varieties or an initialization procedure.